REMARKS

The Official Action mailed July 26, 2002 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for Continued Examination (RCE)* and *Request for One Month Extension of Time*, which extends the shortened statutory period for response to November 26, 2002. Accordingly, Applicant respectfully submits that this response is being timely filed.

Applicants note with appreciation the consideration of the Information Disclosure Statements filed on June 17, 1999; May 30, 2000; October 4, 2000; and September 26, 2001.

Claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52-53, 58-60, 65, 71-73, 75-81 and 100-103 were pending in the present application. New claims 104-121 have been added to recite additional protection to which Applicant is entitled. Claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52-53, 58-60, 65, 71-73, 75-81 and 100-121 are now pending in the present application, of which claims 1-3, 8, 104, 107, 110, 113, 116 and 119 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

Initially, the Examiner's attention is directed to U.S. Patent 6,355,940. Newly added claims 104-121 were drafted in view of claims 1, 2 and 4 of the '940 patent and may recite interfering subject matter. Furthermore, application serial number 09/927,794 is a divisional application based on the '940 patent (Publication Number 2001/0052598 A1), and may still be pending. The Examiner is requested to carefully review the '940 patent and the '794 application in connection with the subject application.

With reference to the Official Action mailed July 26, 2002, paragraph 4 thereof rejects claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52-53, 58-60, 65, 71-73, 75-81 and 100-103 as obvious based on the combination of U.S. Patent 5,403,772 to Zhang et al., U.S. Patent 5,233,447 to Kuribayashi et al., and U.S. Patent 5,173,792 to Matsueda.

As stated in MPEP § 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference

teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

It is respectfully submitted that the Official Action has failed to establish a *prima facie* case of obviousness in that one of skill in the art would not have been motivated to combine the teachings of Zhang, Kuribayashi and Matsueda to achieve the present invention. Specifically, as previously argued, Matsueda discloses TFTs 100A and 100B provided at respective pixel portions of the display device, which is not related to the buffer circuit of the claimed invention. Particularly, it should be noted that Matsueda teaches two parallel-connected TFTs (100A and 100B) in Fig. 7 so that either one of the TFTs can be cut off if it is found to be defective (col. 13, line 57-col. 14, line 13).

In response to this argument, the Official Action asserts that Matsueda teaches that the reliability of a basic control element comprising two or more parallel-connected TFTs is better than that if a basic control element comprising a single TFT. The Official Action thus concludes that one of skill in the art would readily recognize that the reliability of the buffer circuit and/or other peripheral circuits in the active matrix type LC display device of Zhang would also be improved if the basic transistor in the buffer circuit and/or other peripheral circuits is formed of two or more parallel-connected TFTs.

Applicant respectfully disagrees. Matsueda is concerned about a specific problem unique to the pixel portion of an electrooptical display and is silent about the peripheral portion or buffer circuit. Neither Matsueda, nor the other prior art of record, discloses or suggest any problem with the prior art buffer circuit and thus one of skill in

the art would not have been motivated to modify the buffer circuit to include parallel connected TFTs. While the Official Action asserts that such parallel connection would provide greater reliability and thus would be used in a buffer circuit and/or other peripheral circuits, there is no disclosure or suggestion that reliability in such circuits is a problem or that such parallel interconnection of TFTs could solve such problem if it even existed.

As previously noted, the Applicant has recognized a problem in prior art buffer circuits concerning excess heat caused by a large current in the buffer circuit. The present invention is based on a recognition of the problem caused by this excess heat in the buffer circuit, and the Applicants discovered that the problem could be solved when channel-forming regions of at least two transistors are separately provided in at least two separate islands respectively as shown in Fig. 3. Thus, Applicant's have recognized a specific problem that occurs in the buffer circuit and have presented a solution by the present invention.

The Official Action asserts that the fact that Applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. It is respectfully submitted, however, that there is no suggestion in the prior art and, absent the recognition of the problem discovered by Applicant, one of skill in the art would not be motivated to replace the buffer circuit of the prior art with the pixel circuit of Matsueda.

Furthermore, the fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). See MPEP 2143.01. It is respectfully submitted that the teachings of Matsueda are insufficient to teach or suggest to one of skill in the art that the buffer circuit should include parallel connected TFTs. At best, Matsueda teaches that the parallel TFTs could be used in a buffer circuit, not that they should not. See MPEP 2143.01, under the heading *FACT THAT REFERENCES CAN BE COMBINED OR MODIFIED IS NOT SUFFICIENT TO ESTABLISH PRIMA FACIE*

OBVIOUSNESS, wherein it is stated that "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. Reconsideration is requested.

Applicant further respectfully requests the Examiner to contact the undersigned to schedule an interview at a mutually convenient time to further discuss the above matters.

Respectfully submitted,

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